REMARKS

These remarks are in response to the Office Action mailed July 3, 2006 (Office Action). As this reply is timely filed, no fee is believed due. Claims 1, 8, and 15 have been amended to clarify various aspects of the present invention. Support for these amendments can be found throughout the applicants' specification and, more particularly, at paragraphs 3, 4, 24, 25, and 43, as well as in figure 1B. No new matter has been introduced.

In the Office Action, claims 1-21 have been rejected under 35 U.S.C. § 112, second paragraph. The following remarks relate to independent claims 1, 8, and 15. In paragraph "a" of the Office Action, the phrase "modification to a PLD" has been objected to as being "unclear and incomplete as to what is being modified". Claims 1, 8, and 15 have been amended to clarify that the modification is a "user-specified modification to a programmable logic device design that changes a number of components of at least one module of the programmable logic device design".

In paragraph "b" of the Office Action, the phrase "modules of the PLD that have been changed" has been objected to as being "unclear and incomplete as to changing what of the modules". Claims 1, 8, and 15 have been amended to clarify that "each changed module comprises a number of components that is different from the number of components within the module prior to the user-specified modification".

In paragraph "c" of the Office Action, the phrase "unchanged modules" has been objected to as being "incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections". In view of the clarification of a "changed module", applicants believe the phrase "unchanged module" to clearly indicate which modules of the programmable logic device design are referenced, i.e., those that are not "changed" as recited in the claims.

In paragraph "d" of the Office Action, the phrase "floorplanning only the changed modules thereby determining a placement solution that does not violate boundaries of unchanged modules" as being "incomplete for omitting essential steps, such omission amounting to a gap between the steps". Claims 1, 8, and 15 have been

amended to recite "floorplanning only the changed modules of the programmable logic device design without altering boundaries of unchanged modules". The amendment clarifies that only the changed modules are floorplanned and boundaries of unchanged modules are not altered. The changed modules can be floorplanned using any of a variety of techniques as discussed in the specification and further enumerated within the dependent claims.

In light of the amendments and discussion relating to independent claims 1, 8, and 15, withdrawal of the 35 U.S.C. § 112, second paragraph, rejection of claims 1-21 is respectfully requested.

Claims 6-7, 13-14, and 20-21 have been objected to only inasmuch as each is dependent upon a rejected base claim. The Office Action indicates that these claims would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph, and to include all of the limitations of the base claim and any intervening claims. Claims 6 and 20 have been amended to include all limitations of the base claims and any intervening claims. Claim 8 has been amended to include the limitations of claim 13, which has been cancelled. Further claims 6 and 20 have been amended to reflect the changes implemented and discussed herein with reference to the 35 U.S.C. § 112, second paragraph rejections. Claims 7, 14, and 21 have been amended to depend from claims 6, 8, and 20 respectively. Accordingly, claims 6-7, 8, 14, and 20-21 should now be allowable.

Claims 1-5, 8-12, and 15-19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,309,371 to Shikata et al. (Shikata) as well as U.S. Patent No. 6,086,631 to Chaudhary et al. (Chaudhary). With regard to independent claims 1, 8, and 15, the Office Action asserts that both Shikata and Chaudhary teach "receiving a modification to a PLD that has been floorplanned". Claims 1, 8, and 15, as amended, recite "receiving a user-specified modification to a programmable logic device [(PLD)] design that changes a number of components of at least one module of the programmable logic device design, wherein the programmable logic device design has been floorplanned".

Shikata teaches an automated process for circuit block layout for integrated circuits. Chaudhary teaches an automated overlap removal method that can be

applied post-placement. Neither Shikata nor Chaudhary teaches or suggests that a user-specified modification to a PLD design that has been floorplanned can be received.

The Office Action further asserts that Shikata and Chaudhary teach "identifying modules of the PLD that have been changed by the modification". In support, figures 2, 5, 25, and 27 of Shikata and figures 9-11 and 13 of Chaudhary have been cited. Claims 1, 8, and 15 now recite "identifying modules of the programmable logic device design that have been changed by the modification, wherein each changed module comprises a number of components that is different from the number of components within the module prior to the user-specified modification".

As noted, neither Shikata nor Chaudhary teaches or suggests that a user specified modification to a floorplanned PLD design can be received. Further, figures 2, 5, 25, and 27 of Shikata and figures 9-11 and 13 of Chaudhary lack any teaching or suggestion that modules that have been changed by a user-specified modification are distinguished from those that have not. As noted, both references teach automated processes that do not require user input that modifies a module of a floorplanned PLD design.

The Office Action also contends that both Shikata and Chaudhary teach "floorplanning only the changed modules thereby determining a placement solution that does not violate boundaries of unchanged modules". Claims 1, 8, and 15 now recite "floorplanning only the changed modules of the programmable logic device design without altering boundaries of unchanged modules". Again, the applicants note that neither cited reference teaches or suggests that any distinction is made between modules of a PLD design that have been changed by a user-specified modification and those that have not.

In any case, the cited portions of Shikata teach the use of a spring model when laying out blocks of a circuit design and the removal of overlap. With regard to Chaudhary, figures 9-10, 13, 24, 26, and 35 have been cited. The cited figures, however, lack any teaching or suggestion that only changed modules, i.e., modules having a number of components that is different from the number of components

within the module prior to the user-specified modification, of the PLD design are floorplanned while boundaries of unchanged modules remain unaltered.

Regarding claims 2, 9, and 16, the Office Action contends that both Shikata and Chaudhary teach "selecting a shape from a set of shapes for each changed module and assigning each changed module a non-overlapping location on the PLD". In support, the abstract, columns 4, 5, 8, 11, 13, 14, 17, and figures 2, 4-5, 15, 25, and 27 of Shikata have been cited.

The applicants respectfully disagree that Shikata teaches the features recited in claims 2, 9, and 16. In particular Shikata teaches a process by which circuit blocks are configured as circles. Once an initial layout of the circular circuit blocks is performed, the circular circuit blocks are expanded to actual rectangular regions. Shikata does not teach or suggest that a shape is selected from a set of shapes for each changed module or that each changed module is assigned a non-overlapping location on the programmable logic device according to the selected shape of each module as recited in claims 2, 9, and 16. Moreover, as noted, Shikata does not distinguish between changed and unchanged modules as recited in applicants' claims.

Chaudhary also fails to teach or suggest the limitations of claims 2, 9, and 16. Figures 24, 26, and 35 of the Chaudhary specification have been cited in support of the rejection of claims 2, 9, and 16. Applicants reiterate that Chaudhary, like Shikata, does not distinguish between changed and unchanged modules as recited in the claims. Further, figures 24, 26, and 35 do not teach or suggest that a shape is selected from a plurality of shapes for each changed module. Rather, figure 24 teaches replacing individual logic portions (step 2460). Figure 26 teaches modifying the size of overlapping cores (step 2620). Finally, figure 35 teaches "selecting a critical path" (step 3510). The cited portions of Chaudhary are silent with respect to selecting a shape from a plurality of shapes for each changed module.

Claims 3, 10, and 17, which depend from claims 2, 9, and 16 respectively, clarify that shapes are generated for each unchanged module. Again, the cited references do not teach or suggest such a feature.

As neither Shikata nor Chaudhary teaches or suggests the applicants' invention as recited in the claims, withdrawal of the 35 U.S.C. § 102(b) rejections with respect to

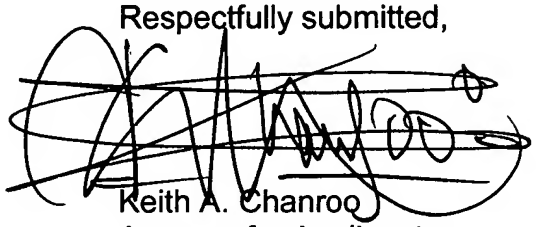
claims 1-5, 8-12, and 15-19 is respectfully requested.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on September 14, 2006.

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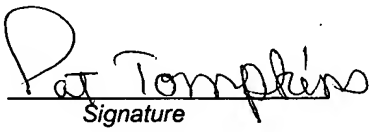

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